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KATTEN MUCHIN ROSENMAN LLP
575 MADISON AVENUE
NEW YORK, NY 10022-2585

EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,249	ZOHAR ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,43,58* is/are allowed.

6)☒ Claim(s) *1-10,12-42,44-57 and 59-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed June 1, 2006 in response to PTO Office Action dated February 23, 2005. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-65 have been presented for examination in this application. In response to the last Office Action, claims 1, 11, 17, 18, 22, 33, 43, 48, 49, and 58 have been amended. Claims 63-65 have been added.

Claim Rejections - 35 USC § 112

Claims 1- 10, 12-42, 44-57, and 59-65 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 recites "...wherein the interim-fast-access-time nodes are configured to be reassignable to a further second range of the LBAs". The Examiner is unaware of any reference in the Specification that teaches this claim limitation. The closest reference appears to be found on page 12, lines 21-23 which outlines that the manager (54) may subsequently reassign the (LBA) ranges during operation. However, this

recitation as well as the Specification as a whole, fails to recite that the nodes are reassigned to a second range of the LBAs, where a send range appears to correspond to respective ranges of LBAs. This argument also applies to independent claims 17, 33, and 48.

Claim 64 recites "... wherein the interim-fast-access-time nodes are configured to be reassigned based on a failure of one of one or more interim-fast-access-time nodes and one or more slow-access-time-mass-storage nodes [col. 5, lines 44-55]. The Examiner is unaware of any reference in the Specification that teaches this claim limitation.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1- rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "...wherein the interim-fast-access-time nodes are configured to be reassignable to a further second range of the LBAs". A limitation directed towards "...respective second range of the LBAs" was previously recited in lines 5-6 and 7. It is unclear whether these respective second ranges are linked to, or correspond to, the "... a further second range of the LBAs" as found in line 11-12.

Claims 64 and 65 recite "...one or more interim-fast-access-time nodes and one or more slow-access-time-mass-storage nodes". It is unclear to the whether these nodes apply to, or correspond to, the "...a plurality of interim-fast-access-time nodes" and "...one or more slow-access-time-storage nodes" as originally claimed in claim 1

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-6, 8-10, 12-22, 24-26, 28-38, 40-42, 44-53, 55-57, and 59-62 are rejected under 35 U.S.C. 102(a) as being anticipated by Henry et al. (US# 6,898,666). The rejections are mode in light of the aforementioned 35 USC, 112, first and second paragraph rejections.

Regarding claim 1, Henry et al. teaches a storage system, comprising: one or more slow-access-time-mass-storage nodes, coupled to store data at respective first ranges of logical block addresses (LBAs) [col. 4, lines 10-23 & 55-67; Fig. 2]; a plurality of interim-fast-access-time nodes [cache pools 1 & 2],configured to operate independently of one another, each interim-fast-access-time node being assigned a respective second range of the LBAs [col. 5, lines 45-55]; and coupled to receive data from and provide data to the one or more slow-access-time-mass-storage nodes having

LBAS within the respective second range [col. 4, lines 55-59]; and one or more interface nodes, which are adapted to receive input/output (I/0) requests from host processors directed to specified LBAS and to direct all the requests to the interim-fast-access-time node to which the specified LBAS are assigned [col. 2, lines 11-15; col. 4, lines 64-67]; wherein the interim-fast-access-time nodes are configured to be reassignable to a further second range of the LBAs [col. 5, lines 44-55; the system is not prevented from being reconfigured in the future to support a different set of LBA values].

Regarding claims 2 and 34, Henry et al. teaches wherein the one or more interface nodes comprise a mapping between the interim-fast-access-time nodes and the LBAS, and wherein the one or more interface nodes are adapted to convert the requests to one or more requests and to direct the one or more requests to respective one or more interim-fast-access-time nodes in response to the mapping [col. 3, lines 39-45; col. 4, lines 55-67].

Regarding claims 3, 19, 35, and 50, Henry et al. teaches wherein the mapping comprises a function [mapping assignment] relating each specific interim-fast-access-time node of the plurality of interim-fast-access-time nodes to the respective second range of the LBAS [col. 3, lines 39-45; col. 4, lines 55-67; col. 5, lines 1-8].

Regarding claim 4, 20, 36, and 51Henry et al. teaches wherein the mapping comprises a table relating each specific interim-fast-access-time node of the plurality of interim-fast-access-time nodes to the respective second range of the LBAS [visually

illustrated in Fig. 5; a broad interpretation of 'table' reads upon the assignment structure of Henry et al.; col. 5, lines 44-55; col. 4, lines 55-67].

Regarding claim 5, 21, 37, and 52, Henry et al. teaches wherein the data is allocated into groups of data within the one or more slow-access-time-mass-storage nodes according to a pre-defined unit of the storage system comprising an integral number of bytes of the data, and wherein the mapping comprises a correspondence between the interim-fast-access-time nodes and the groups of data [col. 5, lines 32-55].

Regarding claim 6, 22, 38, and 53 Henry et al. teaches wherein the one or more slow-access-time-mass-storage nodes comprise one or more disks [Fig. 2], and wherein the interim-fast-access-time nodes comprise random access memories [caches are randomly accessed in accordance with host operations]

Regarding claim 8, 24, 40, and 55, Henry et al. teaches wherein the respective second ranges are spread sufficiently evenly and finely so as to generate well-balanced loading for the plurality of interim-fast-access-time nodes [col. 5, lines 1-8]

Regarding claims 9, 25, 41, and 56, Henry et al. teaches wherein each of the plurality of interim-fast-access-time nodes are at an equal hierarchical level [only one level of cache pool hierarchy; col. 5, lines 9-23].

Regarding claims 10, 26, 42, and 57, Henry et al. teaches wherein the respective second ranges of the LBAS do not overlap [col. 5, lines 5-8].

Regarding claims 12 and 28, Henry et al. teaches wherein the one or more slow-access-time-mass-storage nodes comprise a multiplicity of slow-access-time-mass-storage nodes [multiple disks; Fig. 2] and the respective first ranges are spread sufficiently evenly and finely so as to generate well-balanced loading for the multiplicity [each disk has a range, and that range is mapped to a respective cache pool; col. 5, lines 5-8].

Regarding claims 13, 29, 44, and 59, Henry et al. teaches wherein the plurality of interim-fast-access-time nodes comprises a first interim-fast-access-time node and a second interim-fast-access-time node [cache pool 1, cache pool 2], and wherein the first and second interim-fast-access-time nodes have substantially equal capacities [it is well known in the art that multiple cache systems may be of identical size].

Regarding claims 14, 30, 45, and 60, Henry et al. teaches wherein the plurality of interim-fast-access-time nodes comprises a first interim-fast-access-time node and a second interim-fast-access-time node [cache pool 1, cache pool 2], and wherein the first and second interim-fast-access-time nodes have substantially equal capacities [it is well known in the art that multiple cache systems may be of different sizes].

Regarding claims 15, 31, 46, and 61, Henry et al. teaches wherein the plurality of interim-fast-access-time nodes comprises a first interim-fast-access-time node and a

second interim-fast-access-time node [cache pools 1 &2], and wherein the one or more slow-access-time-mass-storage nodes comprise a first slow-access-time-mass-storage node which is coupled to only receive data from and provide data to the first interim-fast-access-time node and a second slow-access-time-mass-storage node which is coupled to only receive data from and provide data to the second interim-fast-access-time node [each LBA range of each disk is assigned to a specific cache pool; therefore, each disk receives and provides data to a specific cache pool; col. 5, lines 44-55].

Regarding claims 16, 32, 47, and 62, Henry et al. teaches wherein the plurality of interim-fast-access-time nodes comprises a first interim-fast-access-time node and a second interim-fast-access-time node, and wherein the one or more slow-access-time-mass-storage nodes comprise a first slow-access-time-mass-storage node and a second slow-access-time-mass-storage node which are coupled to receive data from and provide data to the first and the second interim-fast-access-time nodes [claim 16 does not specify respective disks that must send and receive data from a specific cache pool; therefore the first disk may send and receive data from the first or second pool while the second disk sends and receives data from the other of the two cache pools; col. 5, lines 44-55].

Regarding claim 17, Henry et al. teaches a method for storing data, comprising: storing the data in one or more slow-access-time-mass-storage nodes having respective first ranges of logical block addresses (LBAs) [col. 4, lines 10-23 & 55-67;

Fig. 2]; assigning to each of a plurality of interim-fast-access-time nodes [cache pools 1 & 2], configured to operate independently of one another, a respective second range of the LBAs [each cache pool is assigned separate LBA ranges for the associated disks; col. 5, lines 45-55]; coupling the plurality of interim-fast-access-time nodes to receive data from and provide data to the one or more slow-access-time-mass-storage nodes having LBAs within the respective second range [col. 4, lines 55-59]; receiving input/output (IO) requests from host processors directed to specified LBAs; and directing all the IO requests to the interim-fast-access-time node to which the specified LBAS are assigned [col. 2, lines 11-15; col. 4, lines 64-67] ; wherein the interim-fast-access-time nodes are configured to be reassignable to a further second range of the LBAs [col. 5, lines 44-55; the system is not prevented from being reconfigured in the future to support a different set of LBA values].

Regarding claims 18 and 49, Henry et al. teaches a storage system according to claim 1, wherein the IO requests are directed to one or more interface nodes, wherein the one or more interface nodes comprise a mapping between the interim-fast-access-time nodes and the LBAS, and wherein the one or more interface nodes are adapted to convert the requests to one or more requests and to direct the one or more requests to respective one or more interim-fast-access-time nodes in response to the mapping [col. 3, lines 39-45; col. 4, lines 55-67].

Regarding claim 22, Henry et al. teaches a method for storing data, comprising: storing the data in one or more slow-access-time-mass-storage nodes having respective first ranges of logical block addresses (LBAs) [col. 4, lines 10-23 & 55-67; Fig. 2]; assigning to each of a plurality of interim-fast-access-time nodes [cache pools 1 & 2], configured to operate independently of one another, a respective second range of the LBAs [each cache pool is assigned separate LBA ranges for the associated disks; col. 5, lines 45-55]; coupling the plurality of interim-fast-access-time nodes to receive data from and provide data to the one or more slow-access-time-mass-storage nodes having LBAs within the respective second range [col. 4, lines 55-59]; receiving input/output (IO) requests from host processors directed to specified LBAs; and directing all the IO requests to the interim-fast-access-time node to which the specified LBAS are assigned [col. 2, lines 11-15; col. 4, lines 64-67], and wherein the interim-fast-access-time nodes comprise random access memories [caches are randomly accessed in accordance with host operations]

Regarding claim 33, Henry et al. teaches a system for transferring data to and from one or more slow-access-time-mass-storage nodes which store data at respective first ranges of logical block addresses (LBAs) [col. 4, lines 10-23 & 55-67; Fig. 2], comprising: a plurality of interim-fast-access-time nodes [cache pools 1 & 2],configured to operate independently of one another, each interim-fast-access-time node being assigned a respective second range of the LBAs [col. 5, lines 45-55]; and coupled to receive data from and provide data to the one or more slow-access-time-mass-storage

nodes having LBAS within the respective second range [col. 4, lines 55-59]; and one or more interface nodes, which are adapted to receive input/output (I/0) requests from host processors directed to specified LBAS and to direct all the requests to the interim-fast-access-time node to which the specified LBAS are assigned [col. 2, lines 11-15; col. 4, lines 64-67] ; wherein the interim-fast-access-time nodes are configured to be reassignable to a further second range of the LBAs [col. 5, lines 44-55; the system is not prevented from being reconfigured in the future to support a different set of LBA values].

Regarding claim 48, Henry et al. teaches a system for transferring data to and from one or more slow-access-time-mass-storage nodes which store data at respective first ranges of logical block addresses (LBAs) [col. 4, lines 10-23 & 55-67; Fig. 2], comprising: assigning to each of a plurality of interim-fast-access-time nodes [cache pools 1 & 2], configured to operate independently of one another, a respective second range of the LBAs [each cache pool is assigned separate LBA ranges for the associated disks; col. 5, lines 45-55]; coupling the plurality of interim-fast-access-time nodes to receive data from and provide data to the one or more slow-access-time-mass-storage nodes having LBAs within the respective second range [col. 4, lines 55-59]; receiving input/output (IO) requests from host processors directed to specified LBAs; and directing all the IO requests to the interim-fast-access-time node to which the specified LBAS are assigned [col. 2, lines 11-15; col. 4, lines 64-67] ; wherein the interim-fast-access-time nodes are configured to be reassignable to a further second range of the

LBAs [col. 5, lines 44-55; the system is not prevented from being reconfigured in the future to support a different set of LBA values].

Regarding claim 63, Henry et al. teaches wherein the interim-fast-access-time nodes are configured to be reassigned by a management node [memory controller; col. 2, lines 11-15].

Regarding claim 65, Henry et al. teaches wherein the interim-fast-access-time nodes are configured to be reassigned based on rebalancing a load between one of one or more interim-fast-access-time nodes and one or more slow-access-time-mass-storage nodes [col. 5, lines 44-55].

Allowable Subject Matter

Claims 11, 43, and 58 are allowed over the prior art of record

Response to Arguments

Applicant's arguments filed 6/1/06 have been fully considered but they are not persuasive.

Regarding Applicant's argument of page 21- 22 that the nodes do not operate independently of one another, the Examiner would like to point out that the pools are independent, but also can access the same areas independently, as noted above in the rejection.

The remainder of the arguments are moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Primary Examiner
Art Unit 2187
August 15, 2006